Notice of Allowability	Application No.	Applicant(s)	
	10/791,193	BEFFA, RAYMOND J.	
	Examiner	Art Unit	
	Ramesh B. Patel	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/21/2005*.

2. ☒ The allowed claim(s) is/are *1-28*.

3. ☒ The drawings filed on *02 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/7/2005
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-28 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art of the record fails to teach or fairly suggest in combination with the other elements and features of the claimed invention regarding claims 1-18 and 22-28, a sorting process used for a plurality of integrated circuit devices for grouping a first plurality of inspected integrated circuit devices of a type having an identification code into a group of integrated circuit devices to undergo a first process and for grouping a second plurality of inspected integrated circuit devices to undergo a second process different than the first process, the process and the method comprising: storing data in association with an individual identification code of each of the integrated circuit devices indicating each of the integrated circuit devices undergoes one of the first process and the second process, said data including at least one of fabrication deviation data, probe data, standard test data, special test data, and enhanced reliability testing data in association with the individual identification code of at least some of the integrated circuit devices; reading the individual identification code of each of the integrated circuit devices; accessing the data stored in association with the individual identification code of each of the integrated circuit devices; and grouping the integrated circuit devices in accordance with the accessed data into those of the plurality of integrated circuit devices to undergo the first process and those integrated circuit devices to undergo the second process and regarding claims 19-21, inspection process for integrated circuit devices from

semiconductor wafers, the method comprising: causing each of the plurality of integrated circuit devices on each of the semiconductor wafers to store an individual identification code; separating each of the plurality of integrated circuit devices on each of the semiconductor wafers forming one of a plurality of integrated circuit devices; storing data in association with the individual identification code associated with each of the plurality of integrated circuit devices that indicates each of the plurality of integrated circuit devices to undergo one of a first process and a second process, storing the data including storing the individual identification code by programming each of the plurality of integrated circuit devices on each of the semiconductor wafers to permanently store a unique fuse identification; reading the individual identification code associated with each of the separated integrated circuit devices; accessing the data stored in association with the individual identification code that is associated with each of the separated integrated circuit devices; grouping each of the plurality of integrated circuit devices in accordance with the accessed data into those integrated circuit devices to undergo the first process and those integrated circuit devices to undergo the second process; and testing the grouped integrated circuit devices using the first process and the second process.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramesh B. Patel whose telephone number is 571-272-3688. The examiner can normally be reached on M-Th; 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ramesh B. Patel
Primary Examiner 4/6/05
Art Unit 2121

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